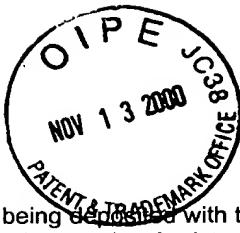


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Docket No.: GR 99 P 4724 US



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By: Jm PDate: 11/8/2000IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Martin Schrems et al.
 Application No. : 09/677,545
 Filed : October 2, 2000
 Title : Trench Capacitor and Method for Fabricating It

*TDS
Chilesen
49-2*

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
 Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

United States Patent No. 4,937,205 (Nakayama et al.), dated June 26, 1990;

United States Patent No. 5,189,503 (Suguro et al.), dated February 23, 1993;

United States Patent No. 5,250,829 (Bronner et al.), dated October 5, 1993;

United States Patent No. 5,344,381 (Cabrera y Lopez Caram), dated September 6, 1994;

Frank S. Becker et al.: "Low Pressure Deposition of Doped SiO₂ by Pyrolysis of Tetraethylorthosilicate (TEOS)", Journal of the Electrochemical Society, Vol. 136, No. 10, October 1989, pp. 3033-3043;

C.N. Ransom et al.: "Shallow n⁺ Junctions in Silicon by Arsenic Gas-Phase Doping", Journal of the Electrochemical Society, Vol. 141, No. 5, May 1994, pp. 1378-1381.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

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For Applicants

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Date: November 8, 2000

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